

Appl. No. 10/691,173

Examiner: TRAN, MAI HUONG C, Art Unit 2818

In response to the Office Action dated March 8, 2005

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AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph at page 3, line 7 with the following rewritten paragraph:

— To achieve the above objects, one aspect of the present invention provides a memory device with vertical transistors and deep trench capacitors. The device includes a substrate containing at least one deep trench and a capacitor deposited in the lower portion of the deep trench. A conducting structure, having a first conductive layer and a second conductive layer, is deposited on the trench capacitor. A ring shaped insulator is deposited on the sidewall and between the substrate and the first conductive layer. The first conductive layer is surrounded by the ring shaped insulator, and the second conductive layer is deposited on the first conductive layer and the ring shaped insulator. A diffusion barrier between the second conductive layer and the substrate of the deep trench is deposited on one side of the sidewall of the deep trench by thermal oxidation. A trench top isolation is deposited on the conducting structure. A control gate, having a control gate layer and a gate dielectric layer, is deposited on the ~~TTO~~ trench top oxide (TTO). A buried strap is deposited within the substrate beside the conducting structure. A doping area is provided within the substrate beside the control gate.